REMARKS

Claims 1-17 stand rejected under 35 U.S.C. §102(e) as being anticipated by Tanaka et al., U.S. Patent No. 6,489,952. Further, claims 1-17 stand rejected under 35 U.S.C. §102(e) as being anticipated by Hasegawa et al., U.S. Patent Application No. 2001/0011979. Applicants traverse these rejections because the references do not disclose or suggest a voltage offset to either a single positive or negative constant level at all times during operation, as recited in all amended independent claims 1, 3, 7, 8, 9, 12 and 17.

The present invention prevents decrease of contrast ratio caused by the incomplete memory effect (when data is maintained in a picture element), and in particular, is concerned with preventing light transmittance in the picture element when data pulses of zero amplitude for displaying "black" are applied to the element. The decrease of contrast ratio is prevented by the use of driving signals which are either positively or negatively offset a single, predetermined value with respect to a reference voltage of the panel, as shown in Figs. 4D1-4D6, which show potentials appearing across each picture element. The amplitude of the single, offset value is selected depending on a desirable variation of contrast ratio of the display panel (page 14, lines 16-24). The offset voltage is one constant value, and it can be either a positive or a negative value. The offset voltage does not change polarity, but is the same offset level at all times of operation when an offset is applied. For example, the single, constant offset value may be +2V at all time frames during operation where an offset is applied.

In Tanaka et al., however, at least two offset values are used since the electrode of Tanaka et al. switches potential from negative to positive throughout the time of operation. Tanaka et al. merely teach two offset values used as part of an inversion driving system, a system in which a direction of an electric field applied to a liquid crystal is inverted at every rewriting of a display screen. Tanaka et al. disclose two distinct levels, a positive level COM2 and a negative level COM1. For this reason, Tanaka et al. do not disclose or suggest a voltage offset to either a single, positive or negative constant level applied at all times during operation where the offset is applied. Withdrawal of this rejection is respectfully requested.

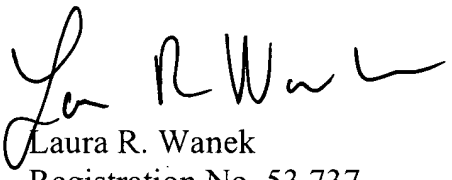
With respect to the Hasegawa et al. reference, the offset voltage is applied to a liquid crystal material during manufacturing or repair of a display, not during operation of the display, as recited in all independent claims of the present invention. In particular, the reference is directed to an alignment treatment for aligning the liquid crystal display, such as when the liquid crystal is destroyed by application of external forces. (paragraph [0088], [0090]). Referring to a sample experiment for an alignment treatment, when a pulse wave was used to apply voltage to the scanning lines, a feedthrough voltage of approximately +1V was generated. The problem of the feedthrough voltage was solved by applying an offset voltage of –1V at the common electrode 17. (paragraph [0117]). Using the offset voltage, "the alignment treatment could be applied and the alignment treatment could be uniformly effected for the entire surface of the image plane...". (paragraph [0118]). Since the offset of Hasegawa is not

used during operation of the display, as required by all independent claims of the present invention, the rejection based on Hasegawa is traversed.

For the foregoing reasons, Applicants believe that this case is in condition for allowance, which is respectfully requested. The Examiner should call Applicants' attorney if an interview would expedite prosecution.

Respectfully submitted,

GREER, BURNS & CRAIN, LTD.

By 
Laura R. Wanek
Registration No. 53,737

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300 South Wacker Drive
Suite 2500
Chicago, Illinois 60606
Telephone: 312.360.0080
Facsimile: 312.360.9315
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